IN THE CLAIMS:

Amend claims 1, 3, 5-7 and 10-12, cancel claims 2, 4, 8, 9 and 13-20 without prejudice or admission, and add new claims 21-23 as shown in the following listing of claims, which replaces all previous listings and versions of claims.

1. A signal processing ~~circuit, comprising~~ circuit comprising:

a sample/hold circuit ~~for sampling~~ that samples an input signal comprised of a first signal and a second signal and for holding the first signal, the first signal comprising an optical signal obtained due to storage of electric charges generated due to light incident upon a photoelectric converter, and the second signal comprising a reference signal obtained due to resetting of the photoelectric converter; ~~separately inputted for a time interval of the first half and for a time interval of the second half for the time interval of the first half and for holding the inputted signal for the time interval of the second half;~~

a subtracter ~~for~~ connected to receive an output signal of the sample/hold circuit and the input signal and for obtaining ~~taking~~ a difference between the output signal of the sample/hold circuit and the input signal; ~~sampled and held signal and the inputted signal;~~ and

a voltage clamp circuit for clamping a part or all of an output signal from the subtracter. ~~receiving as its input a signal from the subtracter,~~

~~wherein the voltage clamp circuit carries out clamping for a part of or all of the time interval of the first half.~~

2. (canceled).

3. (currently amended) A signal processing circuit according to ~~claim 1, further~~ claim 1; wherein the sample/hold circuit comprises a first sample/hold circuit; and further comprising a second sample/hold circuit connected to an output of the voltage clamp circuit for sampling ~~a~~ an output signal ~~from~~ of the voltage clamp circuit when the first sample/hold circuit holds the first ~~for the time interval of the second half to hold the sampled~~ signal.

4. (canceled).

5. (currently amended) A signal processing circuit according to ~~claim 1, wherein~~ claim 1; wherein the subtracter is a differential amplifier comprised of an operational amplifier and a plurality of resistors; and wherein a reference voltage ~~for~~ of the differential amplifier and a ~~subtracter and a first reference voltage used to carry out the~~

clamping voltage of ~~in~~ the voltage clamp circuit are common to each other.

6. (currently amended) An image ~~sensor IC, comprising~~ sensor IC comprising: a ~~the~~ signal processing circuit as claimed in claim ~~2 which is~~ 1 formed together with the photoelectric converter on one semiconductor substrate.

7. (currently amended) An image ~~sensor, comprising~~ sensor comprising: a plurality of image sensor ICs as claimed in claim 6. ~~the signal processing circuit and the photoelectric converter as claimed in claim 2.~~

8. - 9. (canceled)

10. (currently amended) An image sensor ~~IC, comprising~~ IC comprising:

a photoelectric converter;

a signal processing circuit connected to an output terminal ~~for receiving as its input a signal~~ of the photoelectric converter, the signal processing circuit comprising a sample/hold circuit for sampling an input signal comprised of an optical signal and a reference signal and for holding the optical signal, a subtracter connected to receive the output signal of the sample/hold circuit and the input signal and for obtaining a difference between the output signal of the sample/hold circuit and the input signal, and a

voltage clamp circuit for clamping an output signal of the subtracter, the optical signal being obtained due to storage of electric charges generated due to light incident upon the photoelectric converter, and the second signal comprising a reference signal obtained due to resetting of the photoelectric converter;

a signal output terminal connected to an output terminal of the signal processing circuit;

a reference voltage terminal connected to a terminal at which a reference voltage for the signal processing circuit appears;

a reference voltage circuit; and

a resistor ~~provided~~ disposed between the reference voltage circuit and the reference voltage. ~~terminal,~~

~~the signal processing circuit comprising:~~

~~a sample/hold circuit for separately receiving as its input an optical signal and a reference signal for a time interval of the first half and for a time interval of the second half to sample the inputted signal for the time interval of the first half and to hold the sampled signal for the time interval of the second half, wherein the optical signal is obtained due to storage of electric charges generated due to light incident upon a photoelectric conversion area of photoelectric converter and the reference signal is becoming a reference for the photoelectric~~

~~converter;~~

~~a subtracter for taking a difference between the sampled and held signal and the inputted signal; and~~

~~a voltage clamp circuit for clamping a signal from the subtracter for the time interval of the first half,~~

~~wherein one of a reference voltage for the voltage clamp circuit and a reference voltage for the subtracter is supplied through the reference voltage terminal.~~

11. (currently amended) A close contact type image ~~sensor, comprising~~ sensor comprising: a plurality of image sensor ICs ~~each as claimed in claim 10, wherein~~ according to claim 10, the reference voltage terminals of the respective ~~plurality of~~ image sensor ICs ~~are~~ being electrically connected to one another.

12. (currently amended) An image sensor IC according to claim ~~10, further~~ 10; further comprising a gain amplifier for amplifying the output signal clamped ~~signal~~ by the voltage clamp circuit, ~~wherein~~ a reference voltage for the gain amplifier ~~is~~ being supplied through the reference voltage terminal.

13. - 20. (canceled).

21. (new) A signal processing method, comprising the steps of:

generating an input signal comprised of an optical signal component obtained due to storage of electric charges generated due to light incident upon a photoelectric converter and a reference signal component obtained due to resetting of the photoelectric converter;

sampling the input signal and holding the optical signal component of the input signal using a sample/hold circuit;

obtaining a difference between an output signal of the sample/hold circuit and the input signal using a subtracter; and

clamping a part or all of an output signal from the subtracter using a voltage clamp circuit.

22. (new) A signal processing method according to claim 21; further comprising the steps of amplifying the input signal and an output signal from the sample/hold circuit, and inputting the amplified input and output signals to the subtracter.

23. (new) A signal processing method according to claim 21; wherein the sample/hold circuit comprises a first sample/hold circuit; and further comprising the step of sampling an output signal from the voltage clamp circuit using a second sample/hold circuit when the first sample/hold circuit holds the optical signal component.